CLAIMS

What is claimed is:

1. A method for generating a design of an electronic circuit having a plurality of design features, the method comprising the steps of:

storing a plurality of templates, each template including an offset instruction for generating a unique design feature relative to a control point; and

generating at least a portion of the design according to a design instruction file that includes at least one template recall for recalling at least one template, each template recall having control point positioning data for positioning the control point for a respective template relative to a design grid such that a respective unique design feature is generated relative to the control point.

2. The method of claim 1, wherein the plurality of templates includes a template for each of a substantial portion of the unique design features used in a design.

3. The method of claim 1, further comprising the step of creating the design instruction file such that the design instruction file includes a plurality of template recalls, each template recall having a fixed width format.

4. The method of claim 3, wherein each template recall further includes: a template identifier and a net identifier.

5. The method of claim 4, wherein the fixed width format includes 8 bytes for the control point positioning data, and one of 2 and 4 bytes for the template identifier and the same number of bytes for the net identifier as for the template identifier.

6. The method of claim 1, wherein each template includes a polygonal border with a respective control point located at a corner of the polygonal border, and wherein the offset instruction includes data for generating a respective feature relative to the control point.

7. The method of claim 1, wherein the storing step further includes organizing the plurality of templates according to at least one class of feature selected from the group consisting of: circles, arcs, polygons, alphanumeric characters, rectangles, lines and squares.

8. The method of claim 1, further comprising the step of storing a nested feature template including an offset instruction for generating a plurality of unique design features used in a design.

9. A computer-readable medium for storing data for access by an electronic circuit design system executing on a data processing system, the computer-readable medium including a data structure including:

a plurality of data objects, each data object comprising:

a template including an offset instruction for generating a respective design feature relative to a control point.

10. The computer-readable medium of claim 9, wherein the plurality of data objects include a template for each of a substantial portion of the unique design features used in the electronic circuit design.

11. The computer-readable medium of claim 9, wherein each template is recallable by a design instruction file executing on the electronic circuit design system, wherein the design instruction file includes a plurality of template recalls, each template recall having a fixed width format.

12. The computer-readable medium of claim 11, wherein each template recall includes a template identifier, control point positioning data for positioning the control point for a respective template relative to a design grid, and a net identifier.

13. The computer-readable medium of claim 9, wherein each template includes a polygonal border with a respective control point located at a corner of the polygonal border, and wherein

the offset instruction includes data for generating a respective feature relative to the control point.

14. The computer-readable medium of claim 9, wherein the plurality of data objects are organized according to at least one class of feature selected from the group consisting of: circles, arcs, polygons, alphanumeric characters, rectangles, lines and squares.

15. The computer-readable medium of claim 9, wherein the plurality of data objects further include at least one nested template including an offset instruction for generating a plurality of unique design features used in a design.

16. A computer program product comprising a computer useable medium having computer readable program code embodied therein for generating an electronic circuit design, the program product comprising:

program code configured to recall a template for a design feature based on a fixed width format template recall in a design instruction file; and

program code configured to generate the feature based on the template, wherein the template includes an offset instruction for generating the design feature relative to a control point.

17. The program product of claim 16, wherein the template is stored in a database including a plurality of templates, one for each unique feature used in the electronic circuit design.

18. The program product of claim 16, wherein the design instruction file includes a plurality of template recalls, each template recall having a fixed width format.

19. The program product of claim 18, wherein each template recall includes a template identifier and control point positioning data for positioning the control point for a respective template relative to a design grid.

20. A data processing system executing an application program and containing a database used by the application program, the data processing system comprising:

a processor for executing the application program; and

a memory including a data structure accessible by the application program, the data structure comprising:

means for recalling a template for a design feature based on a fixed width format template recall in a design instruction file; and

means for generating the feature based on the template, wherein the template includes an offset instruction for generating the design feature relative to a control point.